**MOORE Machine:**

**Verilog Module:**

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 11:11:39 01/24/2023

// Design Name:

// Module Name: moore\_FSM

// Project Name:

// Target Devices:

// Tool versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module moore\_FSM(Clk,Reset,squence\_in,detector\_out);

input Clk;

input Reset;

input squence\_in;

output detector\_out;

reg detector\_out;

reg [2:0]state;

reg [2:0]next\_state;

parameter [2:0]S0 = 3'b000;

parameter [2:0]S1 = 3'b001;

parameter [2:0]S2 = 3'b010;

parameter [2:0]S3 = 3'b011;

parameter [2:0]S4 = 3'b100;

always@(squence\_in or state) // Next State determination

begin

case(state)

S0:begin

if(squence\_in) begin

next\_state=S1;

end

else begin

next\_state=S0;

end

end

S1:begin

if(squence\_in) begin

next\_state=S1;

end

else begin

next\_state=S2;

end

end

S2:begin

if(squence\_in) begin

next\_state=S3;

end

else begin

next\_state=S0;

end

end

S3:begin

if(squence\_in) begin

next\_state=S4;

end

else begin

next\_state=S2;

end

end

S4:begin

if(squence\_in) begin

next\_state=S1;

end

else begin

next\_state=S2;

end

end

endcase

end

always @(posedge Clk) // State Registers

begin

if(Reset)

begin

state <= S0;

end

else begin

state<=next\_state;

end

end

always@(state) // output determination

begin

case(state)

S0:begin

detector\_out<=0;

end

S1:begin

detector\_out<=0;

end

S2:begin

detector\_out<=0;

end

S3:begin

detector\_out<=0;

end

S4:begin

detector\_out<=1;

end

endcase

end

endmodule

**TexT FIXTURE:**

`timescale 1ns / 1ps

////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 11:17:47 01/24/2023

// Design Name: moore\_FSM

// Module Name: D:/moore\_sequence/testbench.v

// Project Name: moore

// Target Device:

// Tool versions:

// Description:

//

// Verilog Test Fixture created by ISE for module: moore\_FSM

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

////////////////////////////////////////////////////////////////////////////////

module testbench;

// Inputs

reg Clk;

reg Reset;

reg squence\_in;

// Outputs

wire detector\_out;

// Instantiate the Unit Under Test (UUT)

moore\_FSM uut (

.Clk(Clk),

.Reset(Reset),

.squence\_in(squence\_in),

.detector\_out(detector\_out)

);

parameter PERIOD=100;

always

begin

Clk=1;

#(PERIOD/2);

Clk=0;

#(PERIOD/2);

end

// Wait 100 ns for global reset to finish

// Add stimulus here

initial begin

// Initialize Inputs

Reset = 1;

squence\_in = 0;

// Wait 100 ns for global reset to finish

// Add stimulus here

#100; Reset=0;

#100; squence\_in = 1;

#100; squence\_in = 1;

#100; squence\_in = 0;

#100; squence\_in = 1;

#100; squence\_in = 1;

#100; squence\_in = 0;

#100; squence\_in = 0;

#100; squence\_in = 1;

#100; squence\_in = 0;

#100; squence\_in = 1;

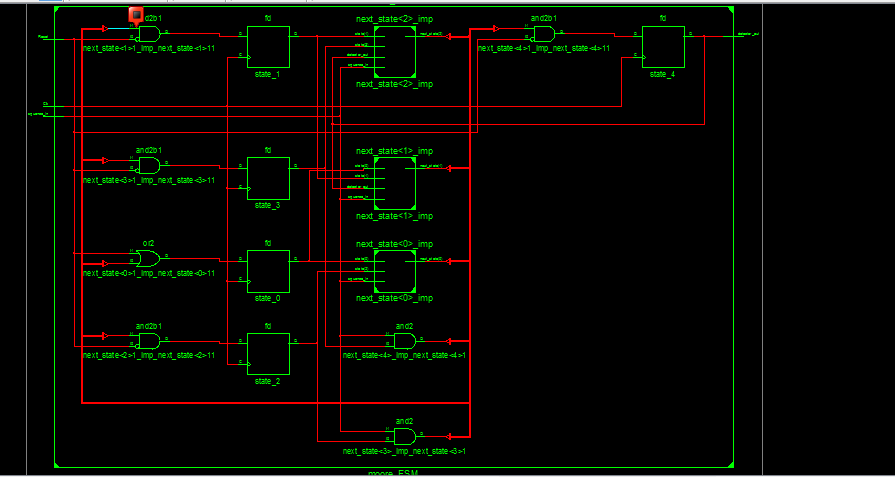
#100; squence\_in = 0;

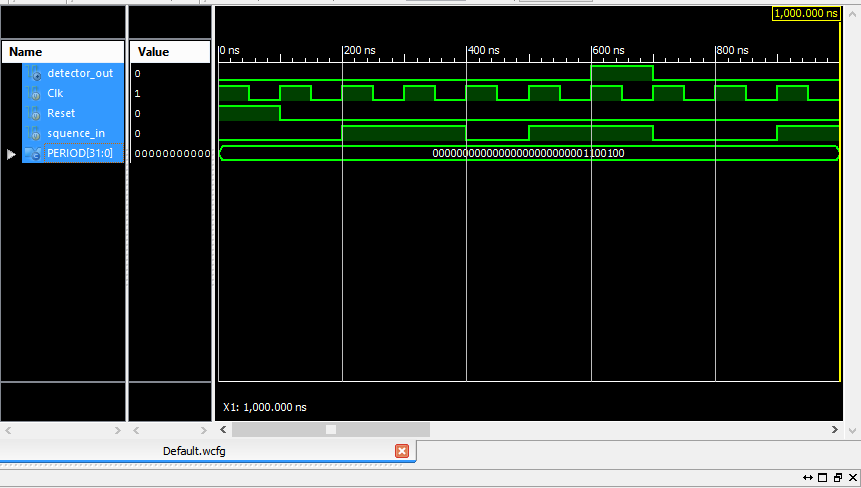
#100; squence\_in = 1;

#100; squence\_in = 1;

end

endmodule

**SCHEMATIC:**

**WAVEFORM:**